# **Rassul Bairamkulov**

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#### Experience

### Postdoctoral scholar

EPFL

• Developing logic synthesis tools for emerging computing technologies

#### **Intern (Design Automation)**

Qualcomm Inc.

- · Automated PCB-level power delivery network layout synthesis in low-power high-performance integrated circuits
- Enables fast PCB prototype generation and comprehensive early power delivery exploration

#### Intern (Power Integrity), Qualcomm Inc.

Qualcomm Inc.

- Developed software to optimize power delivery network parameters based on PPA specifications
- Efficient design space exploration for power delivery in high-performance integrated circuits

#### **Research Assistant**

University of Rochester

- Developed EDA methodologies and software for VLSI power delivery network design, early system-level exploration, and layout synthesis (funded by Qualcomm)
- Developed algorithms and software for clock distribution network synthesis for Superconductive Rapid Single Flux Quantum integrated circuits (funded by Synopsys)
- Developed Infinity Mirror Technique for fast and accurate analysis of voltage drop within large grids (funded by National Science Foundation)

#### **Teaching Assistant**

University of Rochester

• Graduate-level course ECE461 "Introduction to VLSI"

#### **Undergraduate Research Assistant**

Nazarbayev University

• Developed software for minimizing the total harmonic distortion (THD) in multilevel voltage converters

# Education

# University of Rochester

M.S./Ph.D. in Electrical and Computer Engineering

• Thesis title: Graph Algorithms for VLSI Power and Clock Networks

# Nazarbayev University

B.Eng. in Electrical and Electronic Engineering

• Thesis title: Analysis of Natural Voltage Balancing in Single-Phase Multilevel Power Converters

# TECHNICAL SKILLS

Programming	: Python, C++, Matlab/Octave, Mathematica, bash, Verilog
Tools	: HSPICE, Spectre, Cadence Virtuoso, Ansys SIWave, Keysight ADS, Simulink
Languages	: English – fluent, Russian – native, Kazakh – fluent

August 2022 – Present Lausanne, Vaud, Switzerland

May 2020 – August 2020 Remote – Rochester, New York, USA

> May 2018 – August 2018 San Diego, California, USA

June 2017 – June 2022 Rochester, New York, USA

Fall 2017 – Fall 2022 Rochester, New York, USA

November 2014 – May 2016 Astana, Kazakhstan

Rochester, New York, USA June 2016 – June 2022

> Astana, Kazakhstan August 2012 – May 2016

# **Authored Book**

**Bairamkulov, R.** and Friedman, E. G. *Graphs in VLSI*. Springer Nature, Cham, Switzerland, 2023. DOI: 10.1007/978-3-031-11047-4.

## **Journal Articles**

Zhuldassov, N., and **Bairamkulov, R.** and Friedman, E. G. "Thermal Optimization of Hybrid Cryogenic Computing Systems". *IEEE Transactions on Very Large Scale Integration Systems* (early access). DOI: 10.1109/TVLSI.2023.3271898.

**Bairamkulov, R.** and Jabbari, T. and Friedman, E. G. "QuCTS — Single-Flux Quantum Clock Tree Synthesis". *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 41.10 (2021), 3346–3358. DOI: 10.1109/TCAD.2021.3123141.

**Bairamkulov, R.** and Roy, A. and Nagarajan, M. and Srinivas, V. and Friedman, E. G. "SPROUT—Smart Power Routing Tool for Board-Level Exploration and Prototyping". *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 41.7 (2021), 2263–2275. DOI: 10.1109/TCAD.2021.3101411.

**Bairamkulov, R.** and Friedman, E. G. "Effective Resistance of Finite Two-Dimensional Grids Based on Infinity Mirror Technique". *IEEE Transactions on Circuits and Systems I: Regular Papers* 67.9 (2020), 3224–3233. DOI: 10.1109/TCSI.2020.2985652.

**Bairamkulov, R.** and Friedman, E. G. "Effective Resistance of Two-Dimensional Truncated Infinite Mesh Structures". *IEEE Transactions on Circuits and Systems I: Regular Papers* 66.11 (2019), 4368–4376. DOI: 10.1109/TCSI.2019.2933749.

**Bairamkulov, R.** and Xu, K. and Popovich, M. and Ochoa, J. S. and Srinivas, V. and Friedman, E. G. "Power Delivery Exploration Methodology Based on Constrained Optimization". *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 39.9 (2019), 1916–1924. DOI: 10.1109/TCAD.2019.2925397.

## **Conference Proceedings**

**Bairamkulov, R.** and Tempia Calvino, A. and De Micheli, G. "Synthesis of SFQ Circuits with Compound Gates". *To appear in Proceedings of the IEEE/IFIP VLSI-SoC Conference*. 2023.

**Bairamkulov, R.** and De Micheli, G. "Compound Logic Gates for Pipeline Depth Minimization in Single Flux Quantum Integrated Systems". *Proceedings of the ACM Great Lakes Symposium on VLSI*. 2023, 421–425. DOI: 10.1145/3583781.3590287.

**Bairamkulov, R.** and Roy, A. and Nagarajan, M. and Srinivas, V. and Friedman, E. G. "SPROUT—Smart Power Routing Tool for Board-Level Exploration and Prototyping". *Proceedings of the ACM/IEEE Design Automation Conference*. 2021, pp. 283–288. DOI: 10.1109/DAC18074.2021.9586128.

**Bairamkulov, R.** and Friedman, E. G. and Roy, A. and Nagarajan, M. and Srinivas, V. "Graph-Based Power Network Routing for Board-Level High Performance Systems". *Proceedings of the IEEE International Symposium on Circuits and Systems*. 2020, 1–5. DOI: 10.1109/ISCAS45731.2020.9181140.

**Bairamkulov, R.** and Xu, K. and Friedman, E. G. and Popovich, M. and Ochoa, J. and Srinivas, V. "Versatile Framework for Power Delivery Exploration". *Proceedings of the IEEE International Symposium on Circuits and Systems*. 2018, 1–5. DOI: 10.1109/ISCAS.2018.8351478.

**Bairamkulov, R.** and Ruderman, A. and Familiant, Y. L. "Time Domain Optimization of Voltage and Current THD for a Three-Phase Cascaded H-Bridge Inverter". *Proceedings of the IEEE International Power Electronics and Motion Control Conference*. 2016, 227–232. DOI: 10.1109/EPEPEMC.2016.7752002.

## **Doctoral Dissertation**

**Bairamkulov, R.** "Graph Algorithms for VLSI Power and Clock Networks". PhD thesis. University of Rochester, 2022.